

Abstract

ABSTRACT OF THE DISCLOSURE

Method and arrangement for automatically producing clock signals for sampling data signals at different data rates by means of a phase locked loop

- 5 In A method and system for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop, wherein in a synchronization process by means of the phase locked loop (PLL), a data signal (d_s , d_s) is sampled successively using a clock signal (t_s) at different frequencies, which are associated with different transmission protocols, and is checked for the
- 10 presence of protocol identification information ($PID1...n$) associated with the selected clock signal (t_s), until protocol identification information ($PID1...n$) is detected, ~~such that the~~ The frequency resolution of the phase locked loop (PLL) is advantageously increased, and the synchronization of the clock signal (t_s) to the data signal (d_s) is ~~thus~~ improved.

- 15 FIGURE 1